Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ROBERT L. RICHMOND
and PAUL F. WYAR

Appeal No. 1998-0747
Application 08/609,958[1]

ON BRIEF

Before URYNOWICZ, THOMAS and GROSS, Administrative Patent Judges.

URYNOWICZ, Administrative Patent Judge.

## Decision on Appeal

This appeal is from the final rejection of claims 1-18 and 22-31, all the claims pending in the application.

The invention pertains to redundancy switchover control systems. Claim 1 is illustrative and reads as follows:

1. A system comprising:

[1] Application for patent filed March 4, 1996.

a plurality of components, at least one of said components serving as a spare component; and

a plurality of switches connected to the inputs and outputs of said components such that the inputs and outputs of each of said components may be rerouted through said spare component,

wherein each of said plurality of components comprises a single controller for (i) monitoring status information received from the other components, (ii) detecting when one of the other components has failed, and (iii) controlling said switches such that said spare component replaces a failed one of the other components.

The references relied upon by the examiner as evidence of obviousness are:

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| Entenman | 4,245,342 | Jan. 13, 1981 |
| Yajima | 4,709,325 | Nov. 24, 1987 |
| Ozaki | 5,345,438 | Sep. 06, 1994 (filed Aug. 21, 1992) |

Claims 1-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yajima in view of Ozaki.

Claims 3 and 4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yajima in view of Ozaki and Entenman.

Claims 8-18 and 22-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Entenman in view of Ozaki and Yajima.

The respective positions of the examiner and the appellants with regard to the propriety of these rejections are set forth in the examiner’s answer and supplemental answer (Paper Nos. 21 and 24) and the appellants’ brief and reply brief (Paper Nos. 20 and 23).

## Appellants' Invention

Referring to Figure 1, components 20a and 20b, which may be modems, are connected between relay switches 30 and 35. Each component includes an operational element 31, an EPROM 22, a RAM 23

and a summary failure indicator 24, all of which are controlled by a microprocessor 21. A microprocessor determines whether the component is to serve as a spare component or an operating component. If a failure occurs in an operating component such as 20a, the
microprocessor 21b detects a failure signal from the summary failure indicator 24a. The microprocessor 21b then transmits a switch control signal to cause relay switches 30 and 35 to disconnect component 20a from the input and output lines, and connect component 20b to these lines. The microprocessor 21b then enters into an operating mode by executing instructions stored in the EPROM 22b.

## The Prior Art

Yajima discloses a microprocessor system. Referring to Figure 1, assuming a second processor unit 12 fails, a second processor connection circuit $23_2$ sends a fault signal to the first processor unit 11 via the processor interface line 14. The fault signal is detected by the fault detector $43_1$ in the first processor unit, which prompts the first common memory controller $47_1$ to access the second control set saved in the common memory area 32 via the interface controllers 58 and 62 (Figure 6). The first processor unit then processes the second control set to perform the functions of the failed second processor unit.

Entenman discloses a system wherein operating modem modules $10_1$-$10_n$ are physically separated from a redundant spare module 12 (Figure 1). The redundant module 12 is idle until a control system detects a failure in one of the modules 10 and activates the redundant module 12 to operate in its place.

Ozaki teaches a plurality of switches 30-1 and 30-2 in a redundant system to route data from an active unit such as 111' to a spare unit such as 121' when a fault is detected in the active unit.

Opinion

We will not sustain any of the above rejections.

With respect to the rejection of claims 1-7 over Yajima and Ozaki, the examiner indicates at page 5 of the answer that a person having ordinary skill in the art would have been motivated to

combine the switches of Ozaki with Yajima in order to isolate a failed processor unit, such as 12 in Figure 1, from the rest of the circuit until it is repaired and placed back in service. We are not persuaded by this position. It appears from the description of Yajima's apparatus at column 6, line 30, to column 7, line 15, that once a processor unit or component such as 12 has failed, its function is transferred to component 11. While component 11 is performing the function of component 12, component 12 is shut down

and could be repaired and placed back in service without the switches of Ozaki.

As indicated above, the examiner relies on switches in Ozaki to meet the claim recitation of a plurality of switches connected

to the inputs and outputs of the components. However, even if there were motivation to combine Yajima and Ozaki, the combination would not result in the invention set forth in claims 1-7. For example, with respect to Figure 2, Ozaki discloses output switches 30-1 and 30-2, but no input switches. Switches 32-1 and 32-2 operate in conjunction with the output switches and cannot be identified as input switches.

The combination of Entenman with Yajima and Ozaki in the further rejection of dependent claims 3 and 4 will not be sustained for the same reasons that the rejection of claims 1-7 as obvious over Yajima and Ozaki will not be sustained. The examiner merely relied on Entenman to meet the limitations of claims 3 and 4 that the components are modems.

The rejection of claims 8-18 and 22-31 as obvious over Entenman, Yajima and Ozaki will not be sustained for the same reason that the rejection of claims 1-7 over Yajima and Ozaki will not be sustained. No convincing motivation for combining Ozaki with Yajima and Entenman has been established, and independent claims 8, 22 and 24 all define a plurality of switches connected to the inputs and outputs of components or modems.

The following new rejection is entered pursuant to 37 CFR

§ 1.196(b).

Claims 1, 2 and 5-7 are rejected under 35 U.S.C. § 103 as unpatentable over Yajima. With respect to independent claim 1, Yajima's processor units 11 and 12 are a plurality of components, at least one of which serves as a spare component. From column 6, line 30, to column 7, line 15, Yajima teaches that unit 11 takes over unit 12's function when unit 12 experiences a fault. A plurality of switches in the memory connection circuits $24_1$ and $24_2$ and the processor interface section 31 are connected to the inputs and outputs of each of the components. The switches are inherently present in circuits 24 and interface section so as to direct data in and out of the common memory 32 and the control processors $21_1$ and $21_2$ and main memories $22_1$ and $22_2$. A common memory such as 32 provides data as inputs to the processor units 11 and 12 for processing, and receives processed data from the units. The inputs and outputs of each component are the lines between circuits 24 and the processor interface section 31. Inputs and outputs between unit 12 and the common memory 32 may be rerouted through the spare component 11
upon occurrence of a fault in component 12.

With respect to the last paragraph of claim 1 and Yajima's Figure 1, elements $21_1$ and $21_2$ are identified as control processors.
As such, each comprises a single controller of a component 11 or 12. At column 6, lines 37-42, Yajima discloses that occurrence of a fault in component 12 is transmitted as a fault signal from unit 12 to the fault detector $43_1$ in component 11. Accordingly, controller $21_1$ of component 11 monitors the status of information received from
component 12 and detects when that component has failed. As a consequence of this monitoring and detection, controller $21_1$ functions to control the switches of connection circuits 24 and processor interface section 31 such that component 11 replaces failed component 12 (column 6, line 43 to column 7, line 15). At column 8, lines 5-9, Yajima discloses that the processor units may be greater in number than two.

In their reply brief to the new ground of rejection of claims 1-7 as obvious over Yajima and Ozaki in the answer, appellants did not argue that Yajima does not meet the subject matter of dependent claims 2 and 5-7. At pages 5 and 6 of the answer, the examiner made a specific showing as to how the subject matter of

these claims is met by Yajima. Accordingly, these claims fall with claim 1.

Claims 3, 4, 8-18 and 22-31 are rejected under 35 U.S.C. § 103 as unpatentable over Yajima and Entenman. Yajima teaches a redundancy type system of components comprising processing units 11 and 12. Entenman teaches a redundancy system of components comprising modems 10. Whereas modems are processing units, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize Entenman's modems as the processing units in Yajima. Section 103 requires us to presume that the artisan has full knowledge of the prior art in his field of endeavor and the ability to select and utilize knowledge from analogous arts. In re Deminski, 796 F.2d 436, 442, 230 USPQ 313, 315 (Fed. Cir. 1986).

With respect to dependent claims 15-17, the examiner took the position in the answer that it would have been obvious to provide a chassis for housing the modems of Entenman and that the motivation to do so would have been to protect the actual circuitry. We agree. A conclusion of obviousness may be made from common knowledge and common sense of the person of ordinary skill in the art without any specific hint or suggestion in a particular

reference. In re Bozek, 416 F.2d 1385, 1390, 163 USPQ 545, 549 (CCPA 1969).

Summary

(a) None of the examiner's rejections of the claims on appeal under 35 U.S.C. § 103 is sustained;

(b) a new rejection of each of the claims on appeal is entered under 35 U.S.C. § 103.

This decision contains a new ground of rejection pursuant to 37 CFR § 1.196(b)(amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53,131, 53,197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)). 37 CFR § 1.196(b) provides that, "A new ground of rejection shall not be considered final for purposes of judicial review."

37 CFR § 1.196(b) also provides that the appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of proceedings (§ 1.197(c)) as to the rejected claims:

> (1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner. . . .

> (2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record.
> . . .

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

REVERSED - 1.196(b)

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|---|---|---|
| STANLEY M. URYNOWICZ, JR.<br>Administrative Patent Judge | ) | |
| JAMES D. THOMAS<br>Administrative Patent Judge | ) | BOARD OF PATENT<br>APPEALS AND<br>INTERFERENCES |

)
ANITA PELLMAN GROSS )
Administrative Patent Judge )

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